HARDWARE REFERENCE GUIDE

CoM-T335

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Document Revision : 1.0
Release Date : 2015.12.10

Document Revision History

Date	Document Revision	CoM-T335 Version	Changes
2015.12.10	**V1.0**	**V1.0**	

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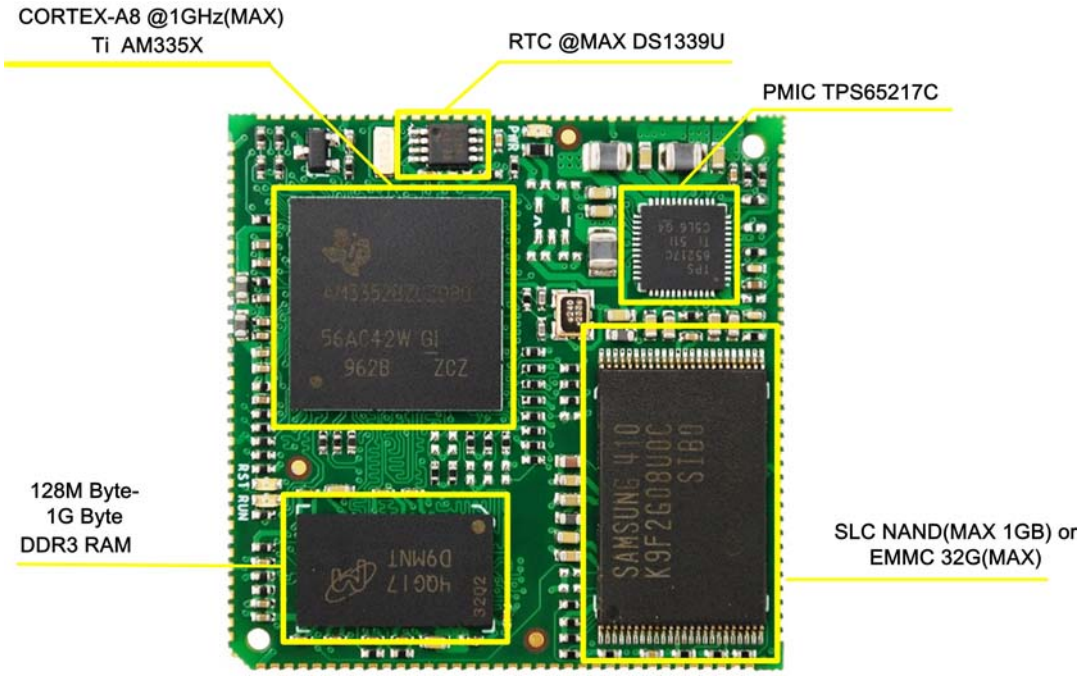
1 Introduction

CoM-T335

Next generation, highly integrated, all-in-one, STAMP SMD computer

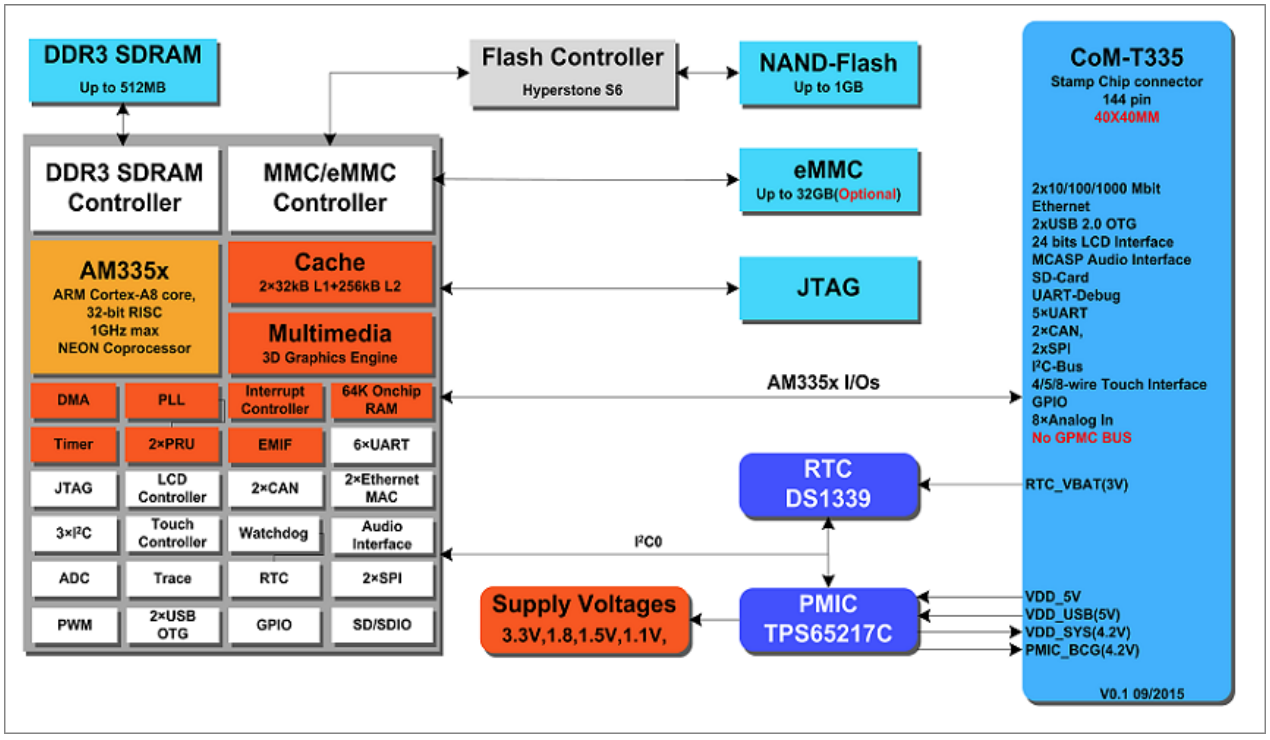
KEY FEATURES

- **Processors from Texas Instruments**
  - Sitara AM335X up to 1GHz Cortex-A8 with NEON SIMD media accelerator
- **Graphics Accelerator**
  - SGX530 2D/3D Graphics Engine up to 20Mpoly/sec (OpenGL 2.0, OpenGL ES 2.0, OpenVG 1.0, Direct3D Mobile and OpenMax support)
- **Memory**
  - Up to 1GB DDR3 SDRAM @ 303Mbps
  - Up to 1GB SLC NAND FLASH (Up to 32GB EMMC optional)
- **Connectivity**
  - 10/100/1000 Mbit support via other on-chip MAC
  - High speed USB2.0 OTG
  - High speed USB2.0 Host
  - UART (6) / SPI (2) / I2C (3)
  - MMC/SD (2)
  - CAN2.0b (x2)
  - External Bus, 16 bit
- **Display and Audio**
  - TFT LCD interface supporting to WXGA (1366x768)
  - Up to 24-bit data output
  - 4-wire Touch screen support
- **Other Peripherals**
  - PWM (x3), Capture (x3) and Encoder (x3) channels
  - Rtc maxiam ds1339 via I2C0
  - Timer (x7) channels
  - 8 channel 12-bit SAR ADC
  - Crypto Hardware accelerators (AES, SHA, PKA, RNG)
  - On board JTAG connector and Boot switch
  - GPIOs : most of CPU pins
- **Boot Options**
  - NAND Flash,SPI Nor Flash, Emmc(iNand) or SD cards
- **Dimension**
  - 40*40 mm STAMP SMD CHIP
  - Miniature size : 40x40 mm
- **Power**
  - Single 5.0V power supply
  - Low power consumption ~1W
- **Temperature**
  - Commercial : 0°C to 70°C
  - Industrial : -40°C to 85°C



Picture of CoM-T335

BLOCK DIAGRAM



PINS ASSIGNMENT

STAMP Pin	CPU Ball	Mode0	Mode1	Mode2	Mode3	Mode4	Modes5	Mode6	Mode7
1	---	GND	---	---	---	---	---	---	---
2	A7	AIN3	---	---	---	---	---	---	---
3	B7	AIN2	---	---	---	---	---	---	---
4	C7	AIN1	---	---	---	---	---	---	---
5	B6	AIN0	---	---	---	---	---	---	---
6	---	GND	---	---	---	---	---	---	---
7	R1	LCD_DATA0	gpmc_a0	pr1_mii_mt0_clk	ehrpwm2A	---	pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio2_6
8	R2	LCD_DATA1	gpmc_a1	pr1_mii0_txen	ehrpwm2B	---	pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio2_7
9	R3	LCD_DATA2	gpmc_a2	pr1_mii0_txd3	ehrpwm2_tripzone	---	pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio2_8
10	R4	LCD_DATA3	gpmc_a3	pr1_mii0_txd2	ehrpwm0_synco	---	pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio2_9
11	T1	LCD_DATA4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in	---	pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2_10
12	T2	LCD_DATA5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in	---	pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2_11
13	T3	LCD_DATA6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2_12
14	T4	LCD_DATA7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2_13
15	U1	LCD_DATA8	gpmc_a12	ehrpwm1_tripzone input	mcasp0_aclkx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	gpio2_14
16	U2	LCD_DATA9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	gpio2_15
17	U3	LCD_DATA10	gpmc_a14	ehrpwm1A	mcasp0_axr0	---	pr1_mii0_rxd1	uart3_ctsn	gpio2_16
18	U4	LCD_DATA11	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	gpio2_17
19	V2	LCD_DATA12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlink	uart4_ctsn	gpio0_8
20	V3	LCD_DATA13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	gpio0_9

STAMP Pin	CPU Ball	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7
21	V4	**LCD_DATA14**	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii_mr0_clk	uart5_ctsn	gpio0_10
22	T5	**LCD_DATA15**	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	gpio0_11
23	---	**GND**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
24	U5	**LCD_VSYNC**	gpmc_a8	**---**	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio2_22
25	R5	**LCD_HSYNC**	gpmc_a9	**---**	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r30_9	pr1_pru1_pru_r31_9	gpio2_23
26	V5	**LCD_PCLK**	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_1	gpio2_24
27	R6	**LCD_AC_BIAS**	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30_11	pr1_pru1_pru_r31_1	gpio2_25
28	U10	GPMC_AD8	lcd_data23	mmc1_dat0	**mmc2_dat4**	ehrpwm2A	pr1_mii_mt0_clk	**---**	gpio0_22
29	T10	GPMC_AD9	lcd_data22	mmc1_dat1	**mmc2_dat5**	ehrpwm2B	pr1_mii0_col	**---**	gpio0_23
30	T11	GPMC_AD10	lcd_data21	mmc1_dat2	**mmc2_dat6**	ehrpwm2_tripzone_i	pr1_mii0_txen	**---**	gpio0_26
31	U12	GPMC_AD11	lcd_data20	mmc1_dat3	**mmc2_dat7**	ehrpwm0_synco	pr1_mii0_txd3	**---**	gpio0_27
32	T12	GPMC_AD12	lcd_data19	mmc1_dat4	**mmc2_dat0**	eQEP2A_in	pr1_mii0_txd2	pr1_pru0_pru_r30_14	gpio1_12
33	R12	GPMC_AD13	lcd_data18	mmc1_dat5	**mmc2_dat1**	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r30_15	gpio1_13
34	V13	GPMC_AD14	lcd_data17	mmc1_dat6	**mmc2_dat2**	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r31_14	gpio1_14
35	U13	GPMC_AD15	lcd_data16	mmc1_dat7	**mmc2_dat3**	eQEP2_strobe	pr1_ecap0_ecap_capin_apwm_o	pr1_pru0_pru_r31_15	gpio1_15
36	---	**GND**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
37	---	**GND**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
38	U9	**GPMC_CS1n**	gpmc_clk	mmc1_clk	pr1_edio_data_in6	pr1_edio_data_out6	pr1_pru1_pru_r30_12	pr1_pru1_pru_r31_12	gpio1_30
39	V9	**GPMC_CS2n**	gpmc_be1n	mmc1_cmd	pr1_edio_data_in7	pr1_edio_data_out7	pr1_pru1_pru_r30_13	pr1_pru1_pru_r31_13	gpio1_31
40	T13	GPMC_CS3n	gpmc_a3	rmii2_crs_dv	**mmc2_cmd**	pr1_mii0_crs	pr1_mdio_data	EMU4	gpio2_0
41	T7	**GPMC_OEn_REn**	timer7	**---**	**---**	**---**	**---**	**---**	gpio2_3
42	U6	**GPMC_WEn**	**---**	timer6	**---**	**---**	**---**	**---**	gpio2_4
43	R7	**GPMC_ADVn_ALE**	**---**	timer4	**---**	**---**	**---**	**---**	gpio2_2

STAMP Pin	CPU Ball	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7
44	T6	**GPMC_BEn0_ CLE**	---	timer5	---	---	---	---	gpio2_5
45	U18	GPMC_BEn1	gmii2_col	gpmc_csn6	mmc2_dat3	gpmc_dir	pr1_mii1_rxlink	mcasp0_aclkr	**gpio1_28**
46	U17	**GPMC_WPN**	GMII2_RXER	GPMC_CSN5	rmii2_rxer	mmc2_sdcd	pr1_mii1_txen	UART4_TXD	gpio0_31
47	T17	**GPMC_WAIT0**	gmii2_crs	gpmc_csn4	rmii2_crs_dv	mmc1_sdcd	pr1_mii1_col	uart4_rxd	gpio0_30
48	V12	GPMC_CLK	lcd_memory_clk	gpmc_wait1	**mmc2_clk**	pr1_mii1_crs	pr1_mdio_mdclk	mcasp0_fsr	gpio2_1
49	---	**GND**	---	---	---	---	---	---	---
50	R13	GPMC_A0	gmii2_txen	**rgmii2_tctl**	rmii2_txen	gpmc_a16	pr1_mii_mt1_clk	ehrpwm1_tripzone_i	gpio1_16
51	V14	GPMC_A1	gmii2_rxdv	**rgmii2_rctl**	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpwm0_synco	gpio1_17
52	U14	GPMC_A2	gmii2_txd3	**rgmii2_td3**	mmc2_dat1	gpmc_a18	pr1_mii1_txd2	ehrpwm1A	gpio1_18
53	T14	GPMC_A3	gmii2_txd2	**rgmii2_td2**	mmc2_dat2	gpmc_a19	pr1_mii1_txd1	ehrpwm1B	gpio1_19
54	R14	GPMC_A4	gmii2_txd1	**rgmii2_td1**	rmii2_txd1	gpmc_a20	pr1_mii1_txd0	eQEP1A_in	gpio1_20
55	V15	GPMC_A5	gmii2_txd0	**rgmii2_td0**	rmii2_txd0	gpmc_a21	pr1_mii1_rxd3	eQEP1B_in	gpio1_21
56	U15	GPMC_A6	gmii2_txclk	**rgmii2_tclk**	mmc2_dat4	gpmc_a22	pr1_mii1_rxd2	eQEP1_index	gpio1_22
57	T15	GPMC_A7	gmii2_rxclk	**rgmii2_rclk**	mmc2_dat5	gpmc_a23	pr1_mii1_rxd1	eQEP1_strobe	gpio1_23
58	V16	GPMC_A8	gmii2_rxd3	**rgmii2_rd3**	mmc2_dat6	gpmc_a24	pr1_mii1_rxd0	mcasp0_aclkx	gpio1_24
59	U16	GPMC_A9	gmii2_rxd2	**rgmii2_rd2**	mmc2_dat7	gpmc_a25	pr1_mii_mr1_clk	mcasp0_fsx	gpio1_25
60	T16	GPMC_A10	gmii2_rxd1	**rgmii2_rd1**	rmii2_rxd1	gpmc_a26	pr1_mii1_rxdv	mcasp0_axr0	gpio1_26
61	V17	GPMC_A11	gmii2_rxd0	**rgmii2_rd0**	rmii2_rxd0	gpmc_a27	pr1_mii1_rxer	mcasp0_axr1	gpio1_27
62	---	**PMIC_PBIN**	---	---	---	---	---	---	---
63	---	**PMIC_LDO4**	---	---	---	---	---	---	---
64	---	**GND**	---	---	---	---	---	---	---
65	---	**PMIC_BCG**	---	---	---	---	---	---	---
66	---	**PMIC_BVS**	---	---	---	---	---	---	---
67	---	**PMIC_BTS**	---	---	---	---	---	---	---

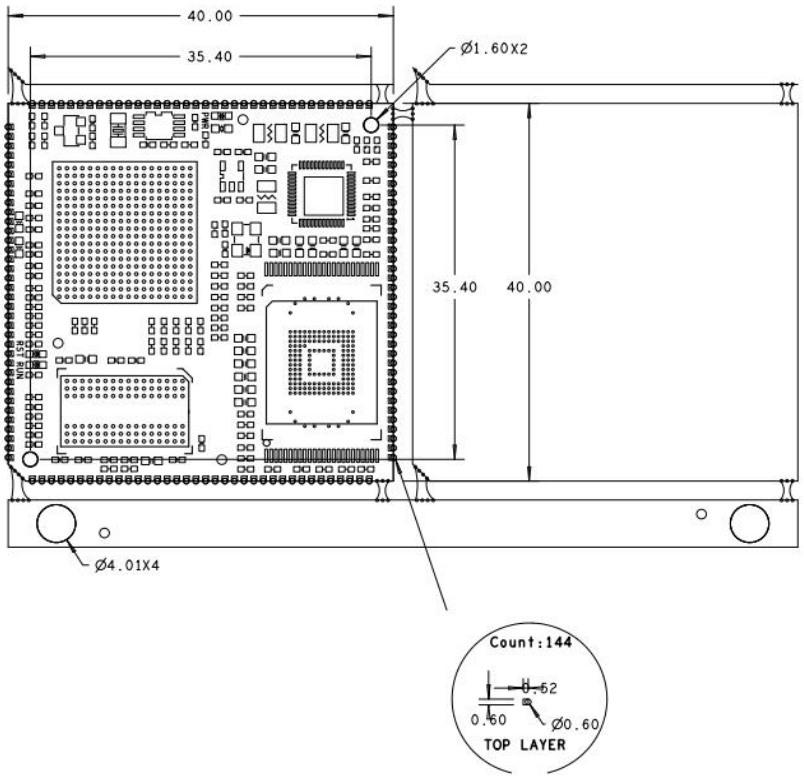
STAMP Pin	CPU Ball	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7
68	---	VDD_SYS_O	---	---	---	---	---	---	---
69	---	VDD_5V_I	---	---	---	---	---	---	---
70	---	GND	---	---	---	---	---	---	---
71	---	VDD_AC_I	---	---	---	---	---	---	---
72	---	VDD_USB_I	---	---	---	---	---	---	---
73	---	GND	---	---	---	---	---	---	---
74	R17	USB1_DP	---	---	---	---	---	---	---
75	R18	USB1_DM	---	---	---	---	---	---	---
76	T18	USB1_VBUS	---	---	---	---	---	---	---
77	F15	USB1_DRVBUS	---	---	---	---	---	---	---
78	N17	USB0_DP	---	---	---	---	---	---	---
79	N18	USB0_DM	---	---	---	---	---	---	---
80	P15	USB0_VBUS	---	---	---	---	---	---	---
81	P16	USB0_ID	---	---	---	---	---	---	---
82	F16	USB0_DRVBUS	---	---	---	---	---	---	---
83	---	GND	---	---	---	---	---	---	---
84	M17	MDIO_DATA	timer6	uart5_rxd	uart3_ctsn	mmc0_sdcd	mmc1_cmd	mmc2_cmd	gpio0_0
85	M18	MDIO_CLK	timer5	uart5_txd	uart3_rtsn	mmc0_sdwp	mmc1_clk	mmc2_clk	gpio0_1
86	M16	gmii1_rxd0	RMII1_RXD0	RGMII1_RD0	mcasp1_ahclkx	mcasp1_ahclkr	mcasp1_aclkr	mcasp0_axr3	gpio2_21
87	L15	gmii1_rxd1	RMII1_RXD1	RGMII1_RD1	mcasp1_axr3	mcasp1_fsr	eQEP0_strobe	mmc2_clk	gpio2_20
88	L16	gmii1_rxd2	UART3_TXD	RGMII1_RD2	mmc0_dat4	mmc1_dat3	uart1_rin	mcasp0_axr1	gpio2_19
89	L17	gmii1_rxd3	UART3_RXD	RGMII1_RD3	mmc0_dat5	mmc1_dat2	uart1_dtrn	mcasp0_axr0	gpio2_18
90	L18	gmii1_rxclk	UART2_TXD	RGMII1_RCLK	mmc0_dat6	mmc1_dat1	uart1_dsrn	mcasp0_fsx	gpio3_10
91	J17	Gmii1_rxdv	lcd_memory_clk	RGMII1_RCTL	uart5_txd	mcasp1_aclkx	mmc2_dat0	mcasp0_aclkr	GPIO3_4

STAMP Pin	CPU Ball	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7
92	H18	RMII1_REFCLK	xdma_event_intr2	spi1_cs0	**UART5_TXD**	mcasp1_axr3	mmc0_pow	mcasp1_ahclkx	gpio0_29
93	K17	gmii1_txd0	RMII1_TXD0	**RGMII1_TD0**	mcasp1_axr2	mcasp1_aclkr	eQEP0B_in	mmc1_clk	gpio0_28
94	K16	gmii1_txd1	RMII1_TXD1	**RGMII1_TD1**	mcasp1_fsr	mcasp1_axr1	eQEP0A_in	mmc1_cmd	gpio0_21
95	K15	gmii1_txd2	DCAN0_RX	**RGMII1_TD2**	uart4_txd	mcasp1_axr0	mmc2_dat2	mcasp0_ahclkx	GPIO0_17
96	J18	gmii1_txd3	DCAN0_TX	**RGMII1_TD3**	uart4_rxd	mcasp1_fsx	mmc2_dat1	mcasp0_fsr	GPIO 0_16
97	K18	gmii1_txclk	UART2_RXD	**RGMII1_TCLK**	mmc0_dat7	mmc1_dat0	uart1_dcdn	mcasp0_aclkx	gpio3_9
98	J16	gmii1_txen	RMII1_TXEN	**RGMII1_TCTL**	timer4	mcasp1_axr0	eQEP0_index	mmc2_cmd	gpio3_3
99	J15	gmii1_rxerr	RMII1_RXERR	spi1_d1	I2C1_SCL	mcasp1_fsx	uart5_rtsn	**UART2_TXD**	gpio3_2
100	H17	gmii1_crs	RMII1_ CRS_DV	spi1_d0	I2C1_SDA	mcasp1_aclkx	uart5_ctsn	**UART2_RXD**	gpio3_1
101	H16	gmii1_col	RMII2_REFCLK	spi1_sclk	**UART5_RXD**	mcasp1_axr2	mmc2_dat3	mcasp0_axr2	GPIO3_0
102	---	**GND**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
103	F17	**MMC0_DAT3**	gpmc_a20	uart4_ctsn	timer5	uart1_dcdn	pr1_pru0_pru_r30_8	pr1_pru0_pru_r31_8	gpio2_26
104	F18	**MMC0_DAT2**	gpmc_a21	uart4_rtsn	timer6	uart1_dsrn	pr1_pru0_pru_r30_9	pr1_pru0_pru_r31_9	gpio2_27
105	G15	**MMC0_DAT1**	gpmc_a22	uart5_ctsn	uart3_rxd	uart1_dtrn	pr1_pru0_pru_r30_10	pr1_pru0_pru_r31_10	gpio2_28
106	G16	**MMC0_DAT0**	gpmc_a23	uart5_rtsn	uart3_txd	uart1_rin	pr1_pru0_pru_r30_11	pr1_pru0_pru_r31_11	gpio2_29
107	G17	**MMC0_CLK**	gpmc_a24	uart3_ctsn	uart2_rxd	dcan1_tx	pr1_pru0_pru_r30_12	pr1_pru0_pru_r31_12	gpio2_30
108	G18	**MMC0_CMD**	gpmc_a25	uart3_rtsn	uart2_txd	dcan1_rx	pr1_pru0_pru_r30_13	pr1_pru0_pru_r31_13	gpio2_31
109	---	**GND**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
110	---	**RTC-VBAT**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
111	A10	**WARMRSTn(nRESETIN_OUT)**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
112	C18	eCAP0_in_PWM0_out	**UART3_TXD**	spi1_cs1	pr1_ecap0_ecap_capin_apwm_o	spi1_sclk	mmc0_sdwp	xdma_event_intr2	GPIO0_7
113	C15	spi0_cs1	**UART3_RXD**	eCAP1_in_PWM1_out	MMC0_POW	xdma_event_intr2	mmc0_sdcd	EMU4	gpio0_6

STAMP Pin	CPU Ball	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7
114	E18	uart0_ctsn	**UART4_RXD**	dcan1_tx	**I2C1_SDA**	spi1_d0	timer7	pr1_edc_sync0_out	gpio1_8
115	E17	Uart0_rtsn	**UART4_TXD**	dcan1_rx	**I2C1_SCL**	spi1_d1	spi1_cs0	pr1_edc_sync1_out	gpio1_9
116	E15	**UART0_RXD**	spi1_cs0	dcan0_tx	I2C2_SDA	eCAP2_in_PWM2_ou	pr1_pru1_pru_r30_14	pr1_pru1_pru_r31_1	gpio1_10
117	E16	**UART0_TXD**	spi1_cs1	dcan0_rx	I2C2_SCL	eCAP1_in_PWM1_ou	pr1_pru1_pru_r30_15	pr1_pru1_pru_r31_1	gpio1_11
118	C17	**I2C0_SDA**	timer4	uart2_ctsn	eCAP2_in_PWM2_out	**---**	**---**	**---**	gpio3_5
119	C16	**I2C0_SCL**	timer7	uart2_rtsn	eCAP1_in_PWM1_out	**---**	**---**	**---**	gpio3_6
120	D18	UART1_CTSn	timer6	dcan0_tx	**I2C2_SDA**	spi1_cs0	pr1_uart0_cts_n	pr1_edc_latch0_in	gpio0_12
121	D17	UART1_RTSn	timer5	dcan0_rx	**I2C2_SCL**	spi1_cs1	pr1_uart0_rts_n	pr1_edc_latch1_in	gpio0_13
122	D16	**UART1_RXD**	mmc1_sdwp	dcan1_tx	I2C1_SDA	---	pr1_uart0_rxd	pr1_pru1_pru_r31_1	gpio0_14
123	D15	**UART1_TXD**	mmc2_sdwp	dcan1_rx	I2C1_SCL	---	pr1_uart0_txd	pr1_pru0_pru_r31_1	gpio0_15
124	A17	SPI0_SCLK	uart2_rxd	I2C2_SDA	ehrpwm0A	pr1_uart0_cts_n	pr1_edio_sof	EMU2	**gpio0_2**
125	B17	SPI0_D0	uart2_txd	I2C2_SCL	ehrpwm0B	pr1_uart0_rts_n	pr1_edio_latch_in	EMU3	**gpio0_3**
126	B16	SPI0_D1	mmc1_sdwp	**I2C1_SDA**	ehrpwm0_tripzone_input	pr1_uart0_rxd	pr1_edio_data_in0	pr1_edio_data_out0	gpio0_4
127	A16	SPI0_CS0	mmc2_sdwp	**I2C1_SCL**	ehrpwm0_synci	pr1_uart0_txd	pr1_edio_data_in1	pr1_edio_data_out1	gpio0_5
128	A15	**XDMA_EVENT_INTR0**	**---**	timer4	clkout1	spi1_cs1	pr1_pru1_pru_r31_16	EMU2	gpio0_19
129	D14	**XDMA_EVENT_INTR1**	**---**	tclkin	clkout2	timer7	pr1_pru0_pru_r31_16	EMU3	gpio0_20
130	---	**GND**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
131	A13	mcasp0_aclkx	ehrpwm0A	**---**	spi1_sclk	mmc0_sdcd	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	**GPIO3_14**
132	B13	mcasp0_fsx	ehrpwm0B	**---**	spi1_d0	mmc1_sdcd	pr1_pru0_pru_r30_1	pr1_pru0_pru_r31_1	**GPIO3_15**
133	D12	mcasp0_axr	ehrpwm0_tripz	**---**	spi1_d1	mmc2_sdcd	pr1_pru0_pru_r30_2	pr1_pru0_pru_r31_2	**GPIO3_16**
134	C12	mcasp0_ahclkr	ehrpwm0_synci	mcasp0_axr2	spi1_cs0	eCAP2_in_PWM2_out	pr1_pru0_pru_r30_3	pr1_pru0_pru_r31_3	**GPIO3_17**

STAMP Pin	CPU Ball	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Mode7
135	B12	mcasp0_aclkr	eQEP0A_in	mcasp0_axr2	**MCASP1_ACLKX**	mmc0_sdwp	pr1_pru0_pru_r30_4	pr1_pru0_pru_r31_4	gpio3_18
136	C13	MCASP0_FSR	eQEP0B_in	mcasp0_axr3	**MCASP1_FSX**	EMU2	pr1_pru0_pru_r30_5	pr1_pru0_pru_r31_5	gpio3_19
137	D13	mcasp0_axr1	eQEP0_index	**---**	**MCASP1_AXR0**	EMU3	pr1_pru0_pru_r30_6	pr1_pru0_pru_r31_6	gpio3_20
138	A14	mcasp0_ahclkx	eQEP0_strobe	mcasp0_axr3	**MCASP1_AXR1**	EMU4	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	gpio3_21
139	---	**GND**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
140	C9	**AIN7**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
141	A8	**AIN6**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
142	B8	**AIN5**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
143	C8	**AIN4**	**---**	**---**	**---**	**---**	**---**	**---**	**---**
144	A9	**GND_ADC**	**---**	**---**	**---**	**---**	**---**	**---**	**---**

CoM-T335 SIZE(mm)



Benefits

- Fast and easy product development
- Power efficient and cost-effective solution
- Reducing your time-to-market
- Ideal for portable, low power and space-constrained products
- Highly integrated computer module
- Multiple connectivity options

TARGET APPLICATIONS

- Industrial applications
- Embedded control
- HMI and Control panels
- Data display systems
- Medical applications
- Building automation
- Hand-held terminals
- Consumer electronics
- Vending Machines

SOFTWARE SUPPORT

- Linux 3.14 and u-Boot (pre-installed)
- WinCE 6.0/7.0 (optional)
- Android 4.0 ICS (optional)
- QT for user interface

2 Functional Description

2.1 Processor

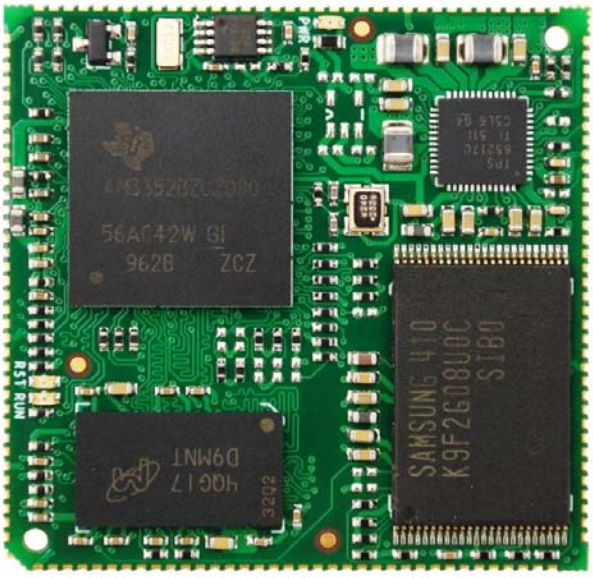
The CoM-T335 is based on Sitara AM335X 1GHz CPU from TI. This microprocessor provides a lot of common features such as:

- ARM Cortex-A8 MPU core, from 300MHz to 1GHz, with NEON multimedia engine
- PowerVR SGX530 2D/3D graphics engine up to 20Mpoly/sec (OpenGL 2.0, OpenGL ES 2.0, OpenVG 1.0, Direct3D Mobile and OpenMax support)
- DDR2/DDR3 controller
- 64KB On-chip RAM
- CPSW, dual 10/100/1000Mbps Ethernet MAC
- Two High speed USB 2.0 OTG
- LCD controller up to 1366x768x24bit color
- Six UART interface
- Three I2C bus interface
- Two SPI interface
- Three MMC SD card support
- Two Multichannel Audio Serial Port (MCASP)
- Two Multichannel Buffered Serial Port (MCBSP)
- 2 x CAN2.0b
- Touch screen controller
- Eight channel 12-bit SAR ADC
- On-chip RTC
- PWM, Timer, Encoder and Capture modules
- Two independent PRU core
- JTAG debug interface

NOTE:

CoM-T335 board has two major categories according to the different ways of storage.One is the flash NAND version, which uses flash NAND to store and boot, the other is the EMMC version, which uses EMMC to store and boot.

EMMC BOOT



NAND FLASH BOOT

NOTE:
There no any EMIFA bus (NOR, SRAM and SDRAM) interface for user that connected to CoM-T335 board.

For more introductions of the processors can be found in the hardware manual.

Since multiplexing of most pins, all peripherals are not available at the same time.

2.2 Memory

2.2.1 DDR3 SDRAM

The CoM-T335 board is assembled with DDR3 SDRAM whose up to 1GB. They are 16-bit, operated with own CS, up to 1GB capacity maximum and clocked at 400MHz (Total data bandwidth is 800Mbps because of DDR).

The DDR3 SDRAM is located in the address range from 0x80000000 to 0xBFFFFFFF for 1GB capacity.

In regard to SDRAM, there are three memory capacities for your choice ,128MB、256MB and 512MB. The following table lists the details.

Capacities	IC	Manufacturer	FBGA Code	Temperature
128MB	K4B1G1646G-BCH9	SAMSUNG	K4B1G1646G-BCH9	0~95℃
	MT41J64M16JT-15E	MICRON	D9MNJ	0~95℃
	MT41J64M16JT-15E IT	MICRON	D9MNT	-40~95℃
256MB	MT41J128M16HA-15E	MICRON	D9LGQ	0~95℃
	K4B2G1646Q-BCK0	SAMSUNG	K4B2G1646Q-BCK0	0~95℃
	MT41J128M16HA-15E IT	MICRON	D9MHD	-40~95℃
512MB	MT41K256M16HA-125	MICRON	D9PXV	0~95℃
	MT41K256M16HA-125 IT	MICRON	D9PZQ	-40~95℃

2.2.2 NAND FLASH

Nand flash is provided to store boot loader, operating system, application data and storage. Samsung Nand flash memory is used in the module. This memory is with 8-bit wide, SLC technology, ONFI compliant and connected to EMIFA controller with CS0 and CS1 to support boot operations. As default the WP# signal is pulled up to enable Program and Erase to operate.

The nand flash needs one or two CS signals that depended on its capacities. The following table shows some common nand flash.

Nand Flash	CS signal
K9F2G08	CSn0
K9K8G08	CSn0
K9WAG08	CSn0,CSn1

- One K9WAG08 and two K9K8G08 are equivalent in capacity. So the K9WAG08 need two CS signals:CS0 and CS1.The STAMP CHIP has three CS signals of GPMC:CSn1、CSn2 and CSn3. If

only nand flash occupies CS0, then there will be three CS signals left to be free. If nand flash occupies two CS signals, then there will be two CS signals left.

For the version of Nand flash, CoM-T335 can choose boot device between Nand flash and SD card by a DIP jumper. For details refer to chapter 3.4.

2.2.3 eMMC

CoM-T335 has an eMMC version. 32GB maximum eMMC (iNand) is provided to store boot loader, operating system, application data or as storage. Sandisk eMMC memory is used for the module. This eMMC uses advanced Multi-Level Cell (MLC) NAND flash technology, enhanced by SanDisk's embedded flash management software which is running as firmware on the flash controller. This memory can be operated in 4bit or 8bit mode.

In the eMMC version, CoM-T335 can choose boot device between eMMC and SD card by a DIP jumper. For details refer to chapter 3.4.

2.3 Peripheral Interfaces

2.3.1 GPMC (General Purpose Memory Controller)

NOTE:

(1) GPMC_AD0- GPMC_AD7 signals are not connect to the stamp chip, So there are no GPMC function for the CoM-T335.

(2) GPMC_CS0n has been used for Nand Flash, so it is not connected to the stamp chip.

The following table shows processor local bus signal descriptions.

Stamp Pin	Signal Name	Type -- Volt.	Description
28	GPMC_AD8	IO 3.3V	GPMC Address Bus & Data Bus
29	GPMC_AD9	IO 3.3V	GPMC Address Bus & Data Bus
30	GPMC_AD10	IO 3.3V	GPMC Address Bus & Data Bus
31	GPMC_AD11	IO 3.3V	GPMC Address Bus & Data Bus
32	GPMC_AD12	IO 3.3V	GPMC Address Bus & Data Bus
33	GPMC_AD13	IO 3.3V	GPMC Address Bus & Data Bus
34	GPMC_AD14	IO 3.3V	GPMC Address Bus & Data Bus
35	GPMC_AD15	IO 3.3V	GPMC Address Bus & Data Bus
38	GPMC_CS1n	O 3.3V	GPMC Chip Select
39	GPMC_CS2n	O 3.3V	GPMC Chip Select

40	GPMC_CS3n	O 3.3V	GPMC Chip Select
41	GPMC_OEn_REn	O 3.3V	GPMC Output / Read Enable

Stamp Pin	Signal Name	Type -- Volt.	Description
42	GPMC_WEn	O 3.3V	GPMC Write Enable
43	GPMC_ADVn_ALE	O 3.3V	GPMC Address Valid / Address Latch Enable
44	GPMC_BEn0_CLE	O 3.3V	GPMC Byte Enable 0 / Command Latch Enable
45	GPMC_BEn1	O 3.3V	GPMC Byte Enable 1
46	GPMC_WPn	O 3.3V	GPMC Write Protect
47	GPMC_WAIT0	O 3.3V	GPMC R/B(Ready or Busy)
48	GPMC_CLK	IO 3.3V	GPMC Clock
50	GPMC_A0	O 3.3V	GPMC Address Bus
51	GPMC_A1	O 3.3V	GPMC Address Bus
52	GPMC_A2	O 3.3V	GPMC Address Bus
53	GPMC_A3	O 3.3V	GPMC Address Bus
54	GPMC_A4	O 3.3V	GPMC Address Bus
55	GPMC_A5	O 3.3V	GPMC Address Bus
56	GPMC_A6	O 3.3V	GPMC Address Bus
57	GPMC_A7	O 3.3V	GPMC Address Bus
58	GPMC_A8	O 3.3V	GPMC Address Bus
59	GPMC_A9	O 3.3V	GPMC Address Bus
60	GPMC_A10	O 3.3V	GPMC Address Bus
61	GPMC_A11	O 3.3V	GPMC Address Bus

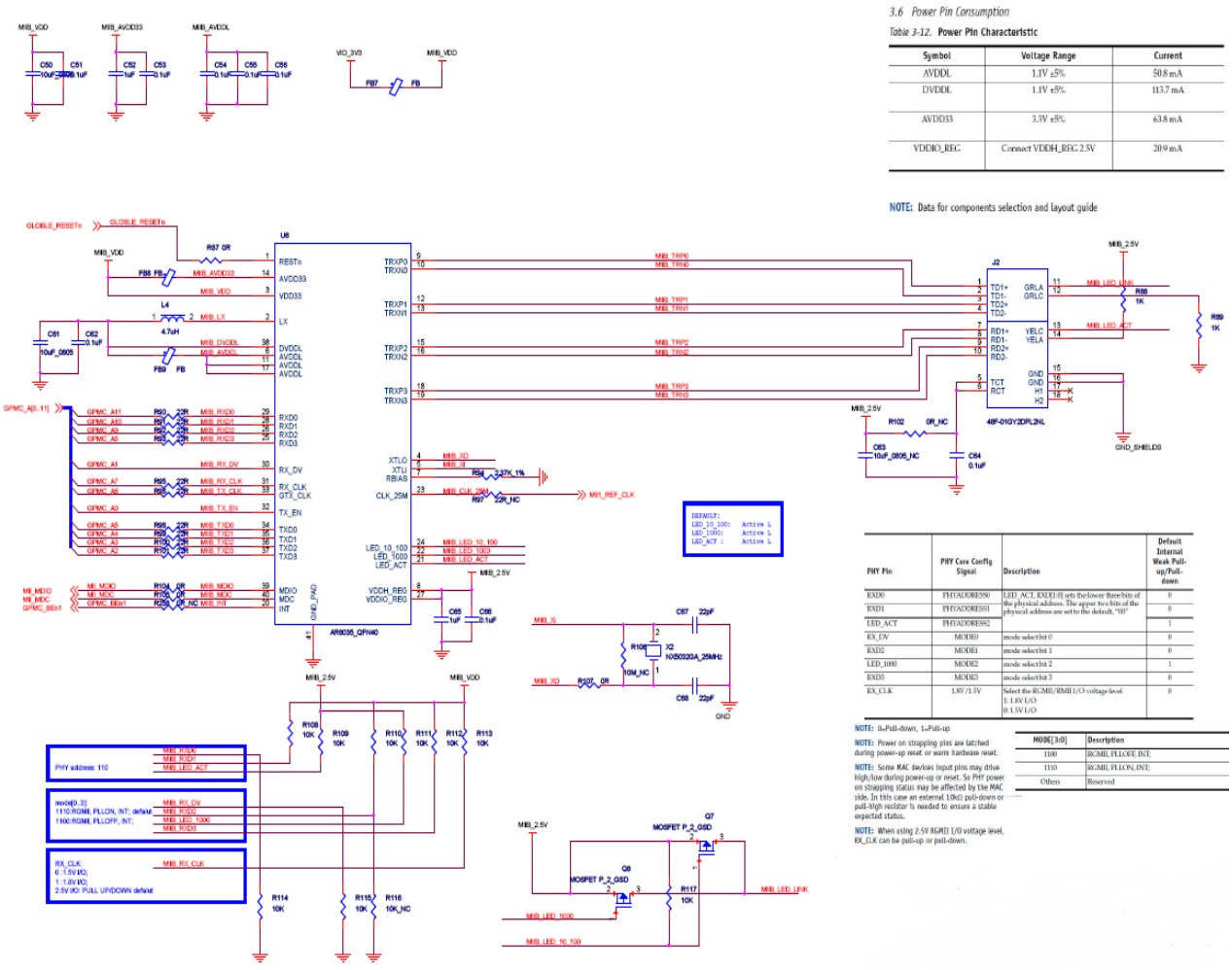
Note:

GPMC bus has four CS signals: GPMC_CS0n, GPMC_CS1n, GPMC_CS2n, and GPMC_CS3n. All of these CS signals are connected to STAMP CHIP except GPMC_CS0n because it is used for nand flash. Since nand flash needs one or two CS signals. So the number of available CS signals is determined by how many CS signals are used for nand flash.

The GPMC bus has 16bit data. But GPMC_D [8:15] share pins of processor with LCD_D [16:23]. So if LCD uses 24bit data, the GPMC only can use 8bit. It is Vice versa.

For the CoM-T335 board of Nand version, the GPMC bus is available. You can use it to

extend some peripherals. For example: the second network interface, connected with DSP. In regard to the application of two network interfaces, please contact us, please send an email to info@embedall.com .
In the eMMC version board, eMMC occupies part of GPMC bus pins, so the rest of GPMC pins can only be used as GPIO.



3.6 Power Pin Consumption

Table 3-12. Power Pin Characteristic

Symbol	Voltage Range	Current
AVDDL	1.1V ±5%	50.8 mA
DVDDL	1.1V ±5%	113.7 mA
AVDD33	3.3V ±5%	63.8 mA
VDDIO_REG	Connect VDDH_REG 2.5V	20.9 mA

NOTE: Data for components selection and layout guide

Address lines of GPMC bus are defined as another network interface

2.3.2 Display Interface

The CoM-T335 display interface is based on the processor's LCD controller. LCD controller supports two independent controllers:

- Raster controller : synchronous interface, up to 1366x768x24bit (8bits per-pixel RGB) for STN, color STN, OLED and TFT panels
- LCD interface display controller (LIDD) : asynchronous (memory-mapped) interface for monochrome character displays

NOTE: Due to AM335X processor errata, please give much more attention to assign color mapping to 18bit or 24bit modes.

LCD_DATA[0..23]	RGB888	RGB565
LCD_DATA0	R3	B3
LCD_DATA1	R4	B4
LCD_DATA2	R5	B5
LCD_DATA3	R6	B6
LCD_DATA4	R7	B7
LCD_DATA5	G2	G2
LCD_DATA6	G3	G3
LCD_DATA7	G4	G4
LCD_DATA8	G5	G5
LCD_DATA9	G6	G6
LCD_DATA10	G7	G7
LCD_DATA11	B3	R3
LCD_DATA12	B4	R4
LCD_DATA13	B5	R5
LCD_DATA14	B6	R6
LCD_DATA15	B7	R7
LCD_DATA16	R2	---
LCD_DATA17	B2	---
LCD_DATA18	G1	---
LCD_DATA19	R1	---
LCD_DATA20	B1	---
LCD_DATA21	R0	---
LCD_DATA22	G0	---
LCD_DATA23	B0	---

The LCD bus including RGB data and control signals are directly routed to the STAMP connector. The following table shows processor local bus signal descriptions.

Stamp Pin	Signal Name	Type--Volt.	Description
7	LCD_DATA0	O 3.3V	LCD Data Bus – 0
8	LCD_DATA1	O 3.3V	LCD Data Bus – 1
9	LCD_DATA2	O 3.3V	LCD Data Bus – 2
10	LCD_DATA3	O 3.3V	LCD Data Bus – 3
11	LCD_DATA4	O 3.3V	LCD Data Bus – 4
12	LCD_DATA5	O 3.3V	LCD Data Bus – 5
13	LCD_DATA6	O 3.3V	LCD Data Bus – 6
14	LCD_DATA7	O 3.3V	LCD Data Bus – 7
15	LCD_DATA8	O 3.3V	LCD Data Bus – 8
16	LCD_DATA9	O 3.3V	LCD Data Bus – 9
17	LCD_DATA10	O 3.3V	LCD Data Bus – 10
18	LCD_DATA11	O 3.3V	LCD Data Bus – 11
19	LCD_DATA12	O 3.3V	LCD Data Bus – 12
20	LCD_DATA13	O 3.3V	LCD Data Bus – 13
21	LCD_DATA14	O 3.3V	LCD Data Bus – 14
22	LCD_DATA15	O 3.3V	LCD Data Bus – 15
35	LCD_DATA16	O 3.3V	LCD Data Bus – 16 (share with GPMC_D15)
34	LCD_DATA17	O 3.3V	LCD Data Bus – 17 (share with GPMC_D14)
33	LCD_DATA18	O 3.3V	LCD Data Bus – 18 (share with GPMC_D13)
32	LCD_DATA19	O 3.3V	LCD Data Bus – 19 (share with GPMC_D12)
31	LCD_DATA20	O 3.3V	LCD Data Bus – 20 (share with GPMC_D11)
30	LCD_DATA21	O 3.3V	LCD Data Bus – 21 (share with GPMC_D10)
29	LCD_DATA22	O 3.3V	LCD Data Bus – 22 (share with GPMC_D9)
28	LCD_DATA23	O 3.3V	LCD Data Bus – 23 (share with GPMC_D8)
27	LCD_AC_ENB_CSn(LCD_DE)	O 3.3V	LCD AC bias enable chip select
26	LCD_CLK	O 3.3V	LCD pixel clock LCD

25	LCD_HSYNC	O 3.3V	LCD horizontal sync
24	LCD_VSYNC	O 3.3V	LCD vertical sync

NOTE: Due to heavy signal multiplexing, these signals can reach alternative functions. Please refer to section of Processor Signal Multiplexing (chapter 3.6) for other modes.